CLAIMS

I claim:

1. A method comprising:

removing a section of a first dielectric layer to create a first well extending from a top surface of the first dielectric layer toward a bottom conductor under the first dielectric layer;

removing a section of the bottom conductor to create a hole extending from the bottom of the first well with a width through the bottom conductor to a second dielectric layer, the hole having a width;

removing a portion of the second dielectric layer to result in an anchor volume under the bottom conductor, the anchor volume being adjacent the hole through the bottom conductor and having a width that is wider than the hole through the bottom conductor;

depositing a conductive material to form a top conductor above the first dielectric layer; and

depositing a conductive material to substantially fill the anchor volume and electrically connect the top conductor with the bottom conductor.

2. The method of claim 1, wherein removing the section of the first dielectric layer comprises removing material from the first dielectric layer with a laser.

3. The method of claim 2, wherein the laser is a CO_2 laser with a wavelength of about 10.6 micrometers.

4. The method of claim 1, wherein the first well extends to the bottom conductor.

5. The method of claim 1, wherein the first well has a width in a range from about 62 micrometers to about 82 micrometers.

6. The method of claim 1, wherein the first well has a width in a range from about 69 micrometers to about 75 micrometers.

7. The method of claim 1, wherein removing the section of the bottom conductor to create the hole comprises removing material from the bottom conductor with a UV laser.

8. The method of claim 7, wherein the UV laser has a wavelength of about 266 nanometers.

9. The method of claim 7, wherein the laser has a pulse width of about 3.5 nanoseconds.

10. The method of claim 7, wherein the hole has a width of about 35 micrometers to about 45 micrometers.

11. The method of claim 10, wherein the width of the anchor volume is in a range of about 69 micrometers to about 75 micrometers.

12. The method of claim 1, wherein the conductive material that forms the top conductor and the conductive material that substantially fills the anchor volume comprise copper.

13. A device, comprising:

a first dielectric layer, the first dielectric layer having side walls that define a first well;

a second dielectric layer with side and bottom walls that define an anchor volume with a width;

a bottom conductor between the first and second dielectric layers, the bottom conductor having side walls that define a via hole extending from the first well to the anchor volume, the via hole having a width smaller than the width of the anchor volume; and

a conductive material that substantially fills the first well, the via hole, and the anchor volume.

14. The device of claim 13, further comprising a top conductor, wherein the conductive material electrically connects the top conductor to the bottom conductor.

15. The device of claim 14, wherein the conductive material and the top conductor comprise copper.

16. The device of claim 13, wherein the first well extends to the bottom conductor.

17. The device of claim 13, wherein the first well has a width in a range from about 62 micrometers to about 82 micrometers.

18. The device of claim 17, wherein the first well has a width in a range from about 69 micrometers to about 75 micrometers.

19. The device of claim 13, wherein the width of the via hole is in a range of about 35 micrometers to about 45 micrometers.

20. The device of claim 13, wherein the width of the anchor volume is in a range of about 69 micrometers to about 75 micrometers.

21. The device of claim 13, wherein the first dielectric layer, the second dielectric layer, the bottom conductor and the conductive material comprise a substrate, and further comprising:

a silicon die;

solder balls connecting the silicon die to the substrate;

a printed circuit board; and

connectors connecting the substrate to the printed circuit board.

22. A method comprising:

forming a first dielectric layer;

forming a bottom conductor on the first dielectric layer;

forming a second dielectric layer on the bottom conductor;

removing a section of the second dielectric layer to form a well;

removing a section of the bottom conductor to result in a via hole;

depositing a conductive material to form a top conductor on the second dielectric layer; and

depositing a conductive material in the well and the via hole to electrically connect the top conductor with the bottom conductor.

23. The method of claim 23, wherein the via hole extends all the way through the bottom conductor.

24. The method of claim 24, further comprising etching the second dielectric layer to result in a volume under the bottom conductor, wherein the volume has at least one overlap section that extends beyond a side wall of the via hole.

25. The method of claim 25, wherein the volume under the bottom conductor is an anchor volume and wherein depositing a conductive material in the well and the via hole to electrically connect the top conductor with the bottom conductor further comprises depositing the conductive material to substantially fill the anchor volume.